

1/5

FIG. 1A

FIRST GENERATION
SINGLE CPU - MULTIPLE LINE CARDS
SINGLE ELECTRICAL BACKPLANE

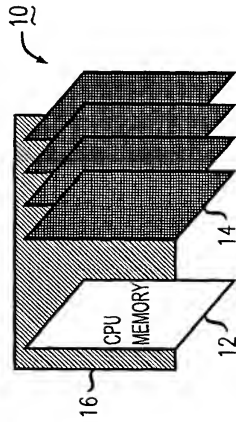


FIG. 1B

SECOND GENERATION
ONE CPU PER LINE CARD
CENTRAL CONTROLLER FOR ROUTING PROTOCOLS

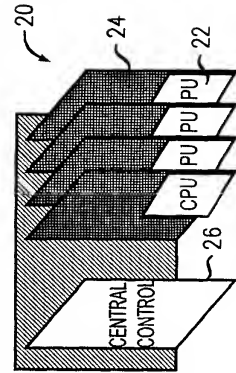


FIG. 1C

THIRD GENERATION
ONE CPU PER LINE CARD CENTRAL
CONTROLLER FOR ROUTING PROTOCOLS
SWITCH FABRIC FOR INTER-CONNECTION

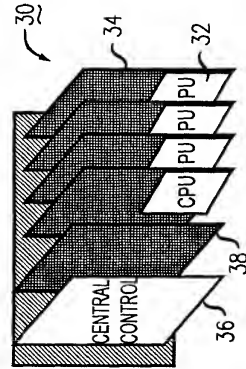
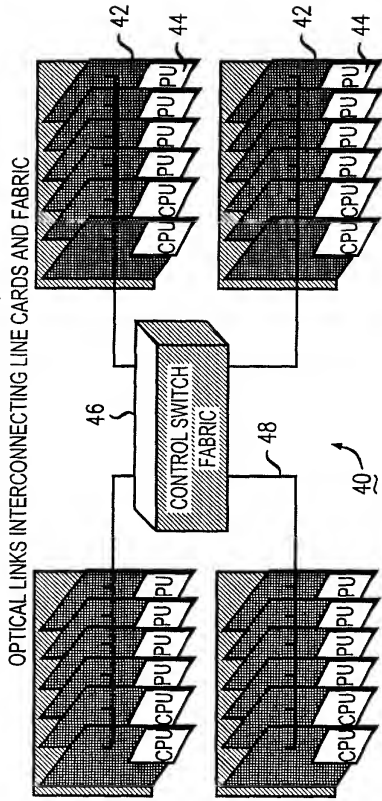


FIG. 1D

FOURTH GENERATION
MULTIPLE SHELVES OF LINE CARDS
CENTRALIZED SWITCH FABRIC
OPTICAL LINKS INTERCONNECTING LINE CARDS AND FABRIC



2/5

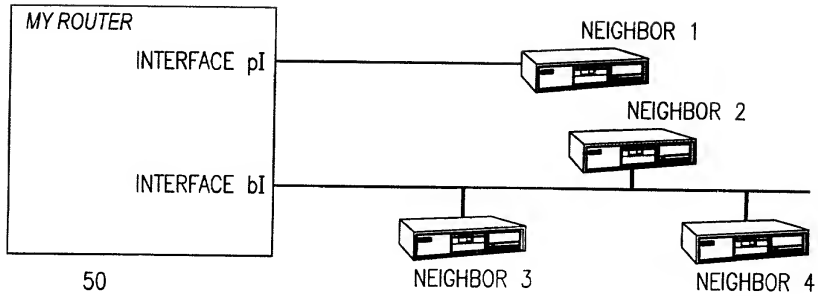


FIG. 2

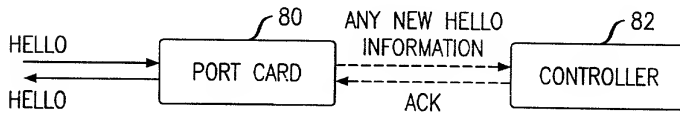


FIG. 5

DISTRIBUTED HELLO PROCESSING

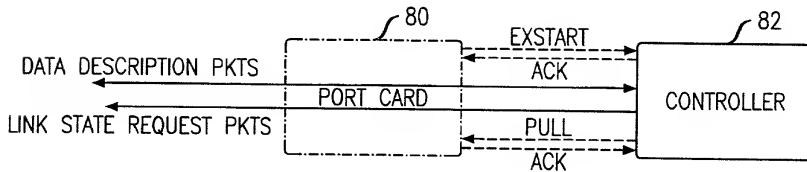


FIG. 6

INITIAL DB EXCHANGE

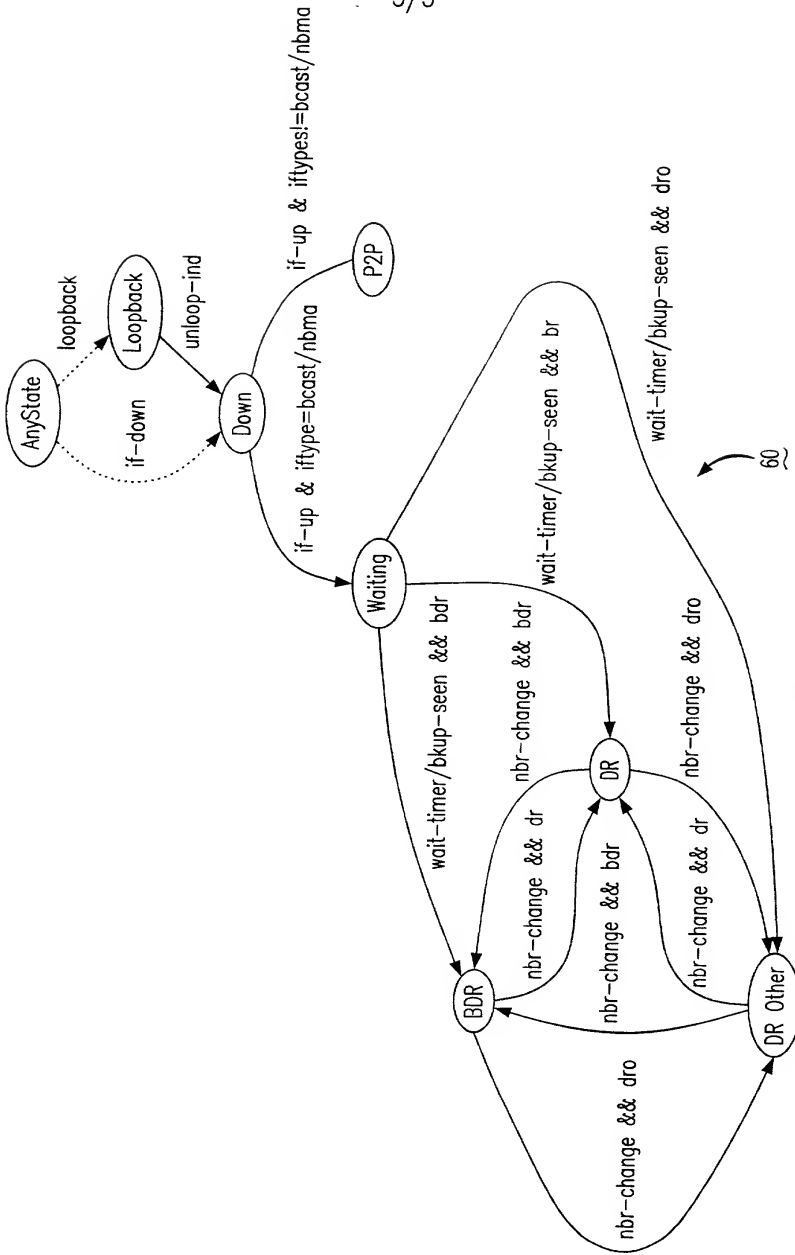


FIG. 3
OSPF INTERFACE FSM

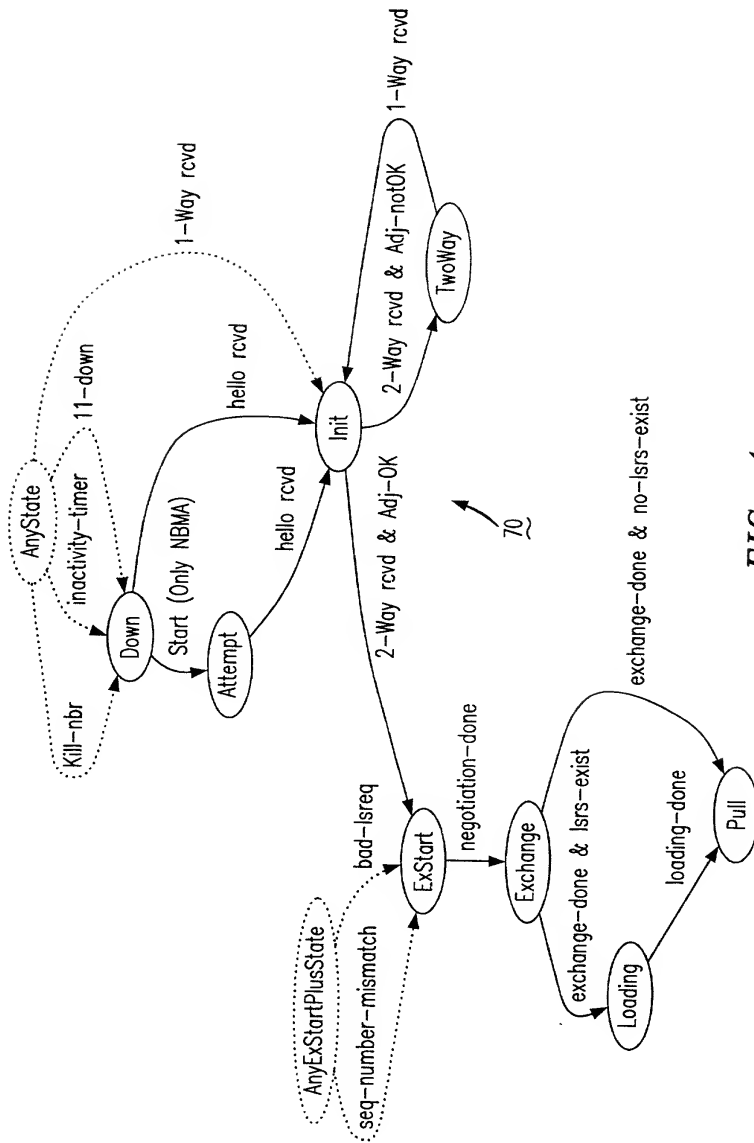


FIG. 4

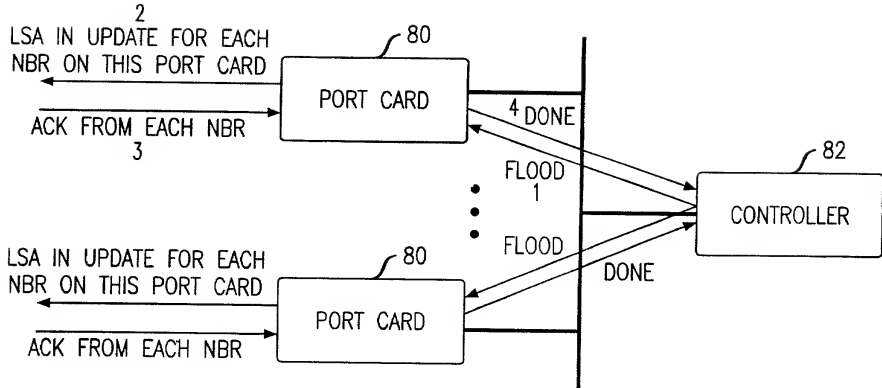


FIG. 7

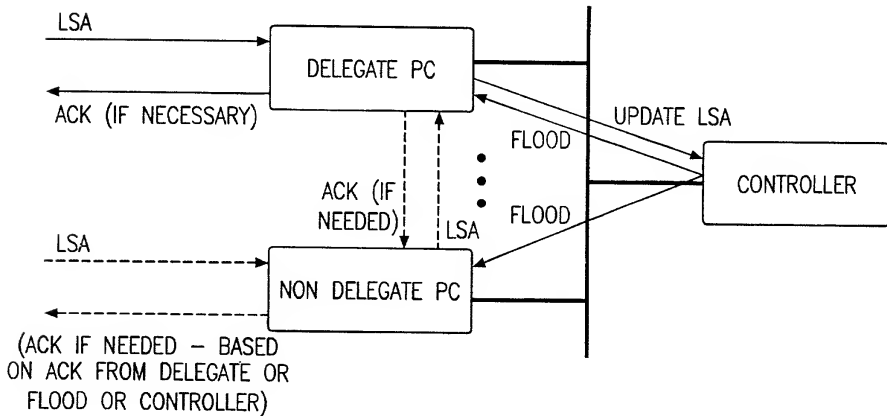


FIG. 8

DISTRIBUTED PROCESSING OF INCOMING LSA UPDATES